

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-235047

(43)Date of publication of application : 10.09.1993

(51)Int.Cl.

H01L 21/338

H01L 29/812

H01L 21/205

(21)Application number : 04-031128

(71)Applicant : NEC CORP

(22)Date of filing : 19.02.1992

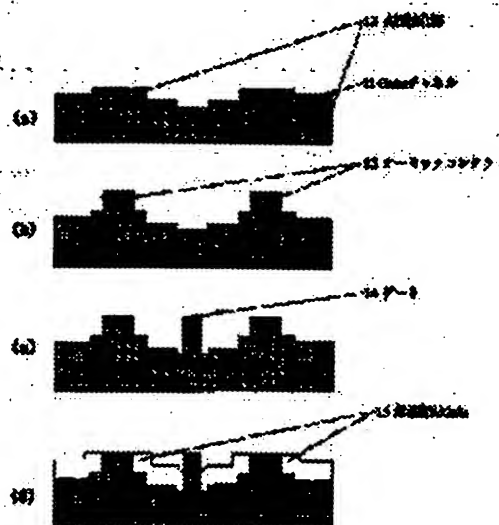
(72)Inventor : IWATA NAOTAKA

(54) MANUFACTURE OF FIELD-EFFECT TRANSISTOR

(57)Abstract:

PURPOSE: To obtain easily a field-effect transistor, which has a high reliability, high breakdown strength, a high output and a high efficiency and moreover, is not subjected to effect of a surface defect level, by a method wherein after a gate electrode is provided on a channel subjected to recess etching, non-doped GaAs layer, an AlGaAs layer or an InAlAs layer is formed.

CONSTITUTION: Boron is ion-implanted in parts other than a channel to form layers 12 having high resistance and after an interelement isolation is performed, a GaAs channel 11 is subjected to mesa etching to a desired form in two stages. An oxide film is formed on the whole surface, a mask for ohmic contact use is applied, the oxide film on the parts of source and drain electrode is opened and after ohmic contacts 13 are formed, a heat treatment is performed. The oxide film on the part of a gate electrode is opened and a gate 14 is formed. Non-doped AlGaAs layers 15 are formed by an atomic layer epitaxial growth method using an organic metal. Thereby, a field-effect transistor having a high reliability, a high output, a high efficiency and a high breakdown strength is obtained.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]